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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
09/960,710	09/19/2001	Bradley L. Taylor	034560-079	4283

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BLAKELY, SOKOLOFF, TAYLOR & ZAFMAN LLP
12400 WILSHIRE BOULEVARD, SEVENTH FLOOR
LOS ANGELES, CA 90025

EXAMINER	
DO, CHAT C	
ART UNIT	PAPER NUMBER
2124	

DATE MAILED: 02/10/2005

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	09/960,710	TAYLOR ET AL.	
	Examiner	Art Unit	
	Chat C. Do	2124	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *19 September 2001 and 22 January 2002 an*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-38* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-38* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *22 January 2002* is/are: a)☐ accepted or b)☒ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date *01/22/02*.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

Drawings

1. The drawings filed on 01/22/2002 are objected to because it is a new set of drawings which are not addressed in the specification. The examiner is examining the application based on the original drawings filed on 09/19/2001. Corrected drawing sheets in compliance with 37 CFR 1.121(d) are required in reply to the Office action to avoid abandonment of the application. Any amended replacement drawing sheet should include all of the figures appearing on the immediate prior version of the sheet, even if only one figure is being amended. The figure or figure number of an amended drawing should not be labeled as "amended." If a drawing figure is to be canceled, the appropriate figure must be removed from the replacement sheet, and where necessary, the remaining figures must be renumbered and appropriate changes made to the brief description of the several views of the drawings for consistency. Additional replacement sheets may be necessary to show the renumbering of the remaining figures. The replacement sheet(s) should be labeled "Replacement Sheet" in the page header (as per 37 CFR 1.84(c)) so as not to obstruct any portion of the drawing figures. If the changes are not accepted by the examiner, the applicant will be notified and informed of any required corrective action in the next Office action. The objection to the drawings will not be held in abeyance.

Claim Objections

2. Claims 10, 18, 23, and 28 are objected to because of the following informalities:

Re claim 10, the applicant is advised to add a period "." at the end of line 6 in the claim to indicate a complete claim.

Re claim 18, the applicant is advised to either amend or cancel this claim because it has exact same limitations cited in claim 8.

Re claim 23, the applicant is advised to either amend or cancel this claim because its limitation is already included or cited in the pre-amble of its preceding claim 19 line 1.

Re claim 28, the applicant is advised to write the word "PN" in full as "pseudo-noise (PN)" in line 3 for clarification.

Appropriate correction is required.

Claim Rejections - 35 USC § 112

3. The following is a quotation of the second paragraph of 35 U.S.C. 112:

> The specification shall conclude with one or more claims particularly pointing out and distinctly claiming the subject matter which the applicant regards as his invention.

4. Claims 2-3, 7, 11, 16, 20, and 28-38 are rejected under 35 U.S.C. 112, second paragraph, as being indefinite for failing to particularly point out and distinctly claim the subject matter which applicant regards as the invention.

Re claim 2, the limitation "a complex half multiplier unit" is unclear whether the complex half multiplier unit means a conventional multi-digit multiplier or just a single bit multiplier. For examination purposes, the examiner considers the complex half multiplier unit as a single bit multiplier. Claims 3, 7, 11, 16, 20, 29, and 32 have the same rejection.

Re claim 28, the limitation "the selectable blocks" in line 3 lacks an antecedence basis. For examination purposes, the examiner considers the limitation as selectable blocks.

Thus, claims 29-38 are also rejected for being dependent on the rejected based claim 28.

Claim Rejections - 35 USC § 102

5. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (e) the invention was described in (1) an application for patent, published under section 122(b), by another filed in the United States before the invention by the applicant for patent or (2) a patent granted on an application for patent by another filed in the United States before the invention by the applicant for patent, except that an international application filed under the treaty defined in section 351(a) shall have the effects for purposes of this subsection of an application filed in the United States only if the international application designated the United States and was published under Article 21(2) of such treaty in the English language.

6. Claims 1-27 are rejected under 35 U.S.C. 102(e) as being anticipated by Abbott (U.S. 6,438,569).

Re claim 1, Abbott discloses in Figures 1 and 7 a reconfigurable chip (e.g. Figure 7B, col. 3 lines 44-53, and col. 29 lines 10-20) comprising: a despreader (e.g. col. 1 lines 40-47) function block including complex multiplier units (e.g. Figure 1A wherein the products are generated by 142-X), the despreader function block including multiplexers (e.g. Figure 1B with mux with CTRL as control signal) to allow the selection of different operation configurations for the despreader function block (e.g. tables 1-2 in cols. 7-8); and interconnect elements (e.g. Figures 1 and particularly Figure 1D wherein all the

bus/link connect all the block together) operably connected to the despreader function block the interconnect elements adapted to selectively connect together the despreader function block with other reconfigurable units (e.g. Figures 7, col. 3 lines 44-53, and col. 29 lines 10-20).

Re claim 2, Abbott further discloses in Figures 1 and 7 the complex multiplier unit comprises a complex half multiplier unit (e.g. Figure 1B wherein the AND gate as half multiplier unit and col. 6 lines 30-40).

Re claim 3, Abbott further discloses in Figures 1 and 7 the complex half multiplier unit comprises a l-bit complex half multiplier unit (e.g. Figure 1B wherein the AND gate as half multiplier unit and col. 6 lines 30-40).

Re claim 4, Abbott further discloses in Figures 1 and 7 the l-bit complex half multiplier is implemented using at least one multiplexer (e.g. MUX in Figure 1B with CTRL signal) and an inverter (e.g. col. 3 lines 7-18 and col. 6 lines 30-40).

Re claim 5, Abbott further discloses in Figures 1 and 7 the despreader function box can also implement a correlation function (e.g. col. 1 lines 40-47).

Re claim 6, Abbott further discloses in Figures 1 and 7 the despreader function block includes a number of despreader trees (e.g. Figure 1A as a tree structure and table 1 is complete tree structures).

Re claim 7, Abbott further discloses in Figures 1 and 7 the despreader trees include a number of complex half multiplier units (e.g. 142-K) connected to adder units (e.g. 148).

Re claim 8, Abbott further discloses in Figures 1 and 7 the despreader function block is controlled by an instruction stored in an associated instruction memory (e.g. Figure 1D with 112 and col. 13 lines 42-47).

Re claim 9, Abbott further discloses in Figures 1 and 7 the despreader function block includes multiple block input multiplexers (e.g. Figures 1A and 1B where the multiplexer exitsing in every generation unit as seen in Figure 1B) and at least one block output multiplexer (e.g. Figure 8).

Re claim 10, it has the same limitations cited in claim 8. Thus, claim 10 is also rejected under the same rationale as cited in the rejection of rejected claim 8.

Re claim 11, it has the same limitations cited in claim 2. Thus, claim 11 is also rejected under the same rationale as cited in the rejection of rejected claim 2.

Re claim 12, it has the same limitations cited in claim 4. Thus, claim 12 is also rejected under the same rationale as cited in the rejection of rejected claim 4.

Re claim 13, it has the same limitations cited in claim 5. Thus, claim 13 is also rejected under the same rationale as cited in the rejection of rejected claim 5.

Re claim 14, Abbott further discloses in Figures 1 and 7 the despreader function block can also implement a multiplication function (e.g. col. 1 lines 30-39 and col. 6 lines 30-40).

Re claim 15, it has the same limitations cited in claim 6. Thus, claim 15 is also rejected under the same rationale as cited in the rejection of rejected claim 6.

Re claim 16, it has the same limitations cited in claim 7. Thus, claim 16 is also rejected under the same rationale as cited in the rejection of rejected claim 7.

Re claim 17, it has the same limitations cited in claim 9. Thus, claim 17 is also rejected under the same rationale as cited in the rejection of rejected claim 9.

Re claim 18, it has the same limitations cited in claim 8. Thus, claim 18 is also rejected under the same rationale as cited in the rejection of rejected claim 8.

Re claim 19, it has the same limitations cited in claim 9. Thus, claim 19 is also rejected under the same rationale as cited in the rejection of rejected claim 9.

Re claim 20, it has the same limitations cited in claim 2. Thus, claim 20 is also rejected under the same rationale as cited in the rejection of rejected claim 2.

Re claim 21, it has the same limitations cited in claim 4. Thus, claim 21 is also rejected under the same rationale as cited in the rejection of rejected claim 4.

Re claim 22, Abbott further discloses in Figures 1 and 7 the despreader tree units further include adder elements (e.g. 148 in Figure 1A).

Re claim 23, it has the same limitations cited in claim 1. Thus, claim 23 is also rejected under the same rationale as cited in the rejection of rejected claim 1.

Re claim 24, it has the same limitations cited in claim 9. Thus, claim 24 is also rejected under the same rationale as cited in the rejection of rejected claim 9.

Re claim 25, Abbott further discloses in Figures 1 and 7 an instruction memory showing multiple instructions for the despreader function block (e.g. Figure 1D with 112, col. 13 lines 40-47).

Re claim 26, it has the same limitations cited in claim 5. Thus, claim 26 is also rejected under the same rationale as cited in the rejection of rejected claim 5.

Re claim 27, it has the same limitations cited in claim 14. Thus, claim 27 is also rejected under the same rationale as cited in the rejection of rejected claim 14.

Claim Rejections - 35 USC § 103

7. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

8. Claims 28-38 are rejected under 35 U.S.C. 103(a) as being obvious over Abbott (U.S. 6,438,569) in view of Black et al. (U.S. 6,661,833).

Re claim 28, Abbott discloses in Figures 1 and 7 a reconfigurable chip comprising: multiple despreader blocks (e.g. Figure 1A), the selectable blocks also being selectable to a non-despreader function (e.g. as correlator as cited in col. 1 line 44); and reconfigurable functional units operably connectable to the despreader blocks, the reconfigurable functional units including an arithmetic logic unit (e.g. sum of product as seen in Figures 1A and 1B). Abbott does not disclose the despreader blocks adapted to despread input signals using an PN sequence. However, Black et al. disclose in Figure 1 the despreader blocks adapted to despread input signals using an PN sequence (e.g. 120). Therefore, it would have been obvious to person having ordinary skill in the art at the time the invention is made to add an PN sequence to utilize in dispreading the input signals as seen in Black et al.'s invention into Abbott's invention because it would enable

to minimize the chance of detecting and intruding the system by outside which enhance the system reliability (col. 2 lines 35-43).

Re claim 29, it has the same limitations cited in claim 2. Thus, claim 29 is also rejected under the same rationale as cited in the rejection of rejected claim 2.

Re claim 30, it has the same limitations cited in claim 4. Thus, claim 30 is also rejected under the same rationale as cited in the rejection of rejected claim 4.

Re claim 31, it has the same limitations cited in claim 6. Thus, claim 31 is also rejected under the same rationale as cited in the rejection of rejected claim 6.

Re claim 32, it has the same limitations cited in claim 7. Thus, claim 32 is also rejected under the same rationale as cited in the rejection of rejected claim 7.

Re claim 33, it has the same limitations cited in claim 5. Thus, claim 33 is also rejected under the same rationale as cited in the rejection of rejected claim 5.

Re claim 34, it has the same limitations cited in claim 14. Thus, claim 34 is also rejected under the same rationale as cited in the rejection of rejected claim 14.

Re claim 35, Abbott further discloses in Figures 1 and 7 interconnect elements (e.g. Figures 1 and particularly Figure 1D wherein all the bus/link connect all the block together) operably connected to the despreader function block the interconnect elements adapted to selectively connect together the despreader function block with other reconfigurable units (e.g. Figures 7, col. 3 lines 44-53, and col. 29 lines 10-20).

Re claim 36, Abbott further discloses in Figures 1 and 7 input multiplexers for the despreader blocks can be selected to connect to operative nearby reconfigurable functional units (e.g. Figures 1B and 5A).

Re claim 37, it has the same limitations cited in claim 9. Thus, claim 37 is also rejected under the same rationale as cited in the rejection of rejected claim 9.

Re claim 38, it has the same limitations cited in claim 25. Thus, claim 38 is also rejected under the same rationale as cited in the rejection of rejected claim 25.

Conclusion

9. The prior art made of record and not relied upon is considered pertinent to applicant's disclosure.

a. U.S. Patent No. 6,449,630 to Bao discloses a multiple function processing core for communication signals.

b. U.S. Patent No. 6,675,187 to Greenberger discloses a pipelined linear array of processor elements for performing matrix computations.

c. U.S. Patent No. 4,811,210 to McAulay discloses a plurality of optical crossbar switches and exchange switches for parallel processor computer.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Chat C. Do whose telephone number is (571) 272-3721. The examiner can normally be reached on M => F from 7:00 AM to 5:30 PM.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Chaki Kakali can be reached on (571) 272-3719. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

Chat C. Do
Examiner
Art Unit 2124

January 25, 2005

KAKALI CHAKI
SUPERVISORY PATENT EXAMINER
TECHNOLOGY CENTER 2100